IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	James deBlanc, et al.	Examiner: Jerry T. Rahll
Serial No.:	10/646,572	Group Art Unit: 2874
Filed:	August 23, 2003	Docket No.: 200206163-1
Title:	Planar Layer with Optical Path	

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is filed in response to the Final Office Action mailed August 10, 2007 and Notice of Appeal filed on November 12, 2007.

AUTHORIZATION TO DEBIT ACCOUNT

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's deposit account no. 08-2025.

I. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no known related appeals, judicial proceedings, or interferences known to appellant, the appellant's legal representative, or assignee that will directly affect or be directly affected by or have a bearing on the Appeal Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1 – 23 and 50 are pending in the application and stand finally rejected. Claims 24 – 49 were canceled. The rejection of claims 1 – 23 and 50 is appealed.

IV. STATUS OF AMENDMENTS

No amendments were made after receipt of the Final Office Action. All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. Note that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element or that these are the sole sources in the specification supporting the claim features.

Claim 1

A method of forming an optical communication path, comprising (Figure 13 illustrates a method of forming an optical cross connect; and Figure 14 illustrates an optical cross connect for selectively coupling otherwise distinct optical paths.):

a) creating a channel (Fig. 14, #1412) within a planar layer (Fig. 14, #1410) in a first substrate of a multi-layered printed circuit board (PCB) (examples of multi-layered PCBs in Figs. 3, 7, and 14) and within a planar layer (Fig. 14, #1430) in a second substrate of the multi-layered PCB (Fig. 13, #1310 and 1320: Fig. 13 shows providing a first planar layer having a plurality (*m*) of optical paths formed within the first planar layer. A second planar layer having a plurality (*n*) of optical paths formed within the second planar layer is provided in step 1320. See p. 12, lines 6-10);

b) forming at least a portion of an optical path within the channel of the first and second substrates, the first and second substrates being stacked together in the multi-layered PCB (Fig. 14 shows the two substrates 1410 and 1430 being vertically stacked. See also Fig. 9, #940: stacking planar layers together to form a multi-layer board: p. 8, lines 4-5); and

c) optically coupling with a switch (Fig. 14, #1424) the channel in the first substrate with the channel in the second substrate (Fig. 13, #1340: the optical switch array is disposed between the first and second planar layers. The first and second planar layers and the switches of the optical switch array are positioned so that the optical

switches enable optically coupling any optical path of the first planar layer with any optical path of the second planar layer: see p. 12, lines 12-16).

Claim 16

A method of forming an optical communication path, comprising (Figure 11 shows a method of forming an optical path with a composite channel. Fig. 7 shows a via insert connecting a plurality of optical paths disposed within distinct planar layers.):

a) providing a first substrate with a first planar layer (Fig. 11, #1160) having a channeled face defining a first channel (Fig. 11, #1162) formed in the first substrate (Fig. 11, #1110: a first planar layer 1160 has a channel face defining a first channel: see p. 9, lines 5-7);

b) providing a second substrate with a second planar layer (Fig. 11, #1170) having a complementary channeled face defining a second channel (Fig. 11, #1172) formed in the second substrate (Fig. 11, #1120: a second planar layer has a complementary channel face that defines a second channel: see p. 9, lines 10-13);

c) placing the first and second planar layers such that the first and complementary second channels oppose each other to form a composite channel defining the optical path in a multi-layered printed circuit board (Fig. 11, #1150: the two planar layers are positioned complimentary of each other such that opposing channels form a single channel: see p. 9, lines 13-15); and

d) providing vias (Fig. 7, #750) through the first and second planar layers to connect the composite channel with different optical pathways extending through different vertically stacked layers of the multi-layered printed circuit board (vias are used to connect to two different channels: see p. 10, lines 11-16; see also Fig. 7 showing a via 750 connecting optical channels in different planar layers).

Claim 50

The method of claim 1 further comprising:

d) switching the switch between an opaque state that prevents passage of an optical signal and a transparent state that permits passage of the optical signal (In the transparent state, an optical switch permits an optical signal to pass through the switch.

In the opaque state, an optical switch substantially eliminates prevents passage of an optical signal through the switch. See p. 13, lines 4-8.).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 and 50 are rejected under 35 USC § 102(b) as being anticipated by USPN 5,432,873 (Hosoya).

Claims 2, 4-5, and 9-11 are rejected under 35 USC § 103(a) as being unpatentable over Hosoya in view of US publication number 2003/0118310 (Steinberg).

Claims 2-5 and 12-15 are rejected under 35 USC § 103(a) as being unpatentable over Hosoya in view of USPN 6,624,077 (White).

Claims 2, 6-9, and 14 are rejected under 35 USC § 103(a) as being unpatentable over Hosoya in view of US publication number 2001/0026670 (Takizawa).

Claims 16, 18-19, and 21-23 are rejected under 35 USC § 103(a) as being unpatentable over USPN 6,624,077 (White) in view of USPN 6,693,736 (Yoshimura).

Claims 17 and 20 are rejected under 35 USC § 103(a) as being unpatentable over USPN 6,624,077 (White) in view of USPN 6,693,736 (Yoshimura) and 2003/0118310 (Steinberg).

VII. ARGUMENT

The rejection of claims 1 – 23 and 50 is improper, and Applicants respectfully request reversal of these rejections.

The claims do not stand or fall together. Instead, Applicants present separate arguments for various claims. Each of these arguments is separately argued below and presented with separate headings and sub-heading as required by 37 C.F.R. § 41.37(c)(1)(vii).

Overview of Claims and Primary References (Hosoya and White)

As a precursor to the arguments, Applicants provide an overview of the claims and the primary references (Hosoya and White). This overview will assist in determining the scope and content of the prior art as required in Graham (see *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 setting out an objective analysis for applying 103 rejections).

Hosoya teaches optical switches with optical waveguides that are formed on top of a substrate, not within the substrates. Figures 1 and 2 of Hosoya show a substrate 6 that has two waveguides 8 and 11 formed on top of the substrate 6. Other embodiments of Hosoya reinforce the teaching that the optical waveguides are formed above the substrate. For example, Figs. 3 – 10 in Hosoya each show a substrate 6 with optical waveguides (8, 11, 22, 23) all formed above the substrate in a separate layer.

White teaches a method for forming an optical waveguide. Fig. 2A in White shows a waveguide 200 having a top substrate 203 and a bottom substrate 204. Two cladding layers 205 and 207 are disposed between the two substrates. A conductive core 210 is disposed in the cladding layers, not in the substrates. White expressly teaches that the channels are formed in a cladding layer, not in a substrate layer.

The claims of the present invention are directed to methods of forming optical communication channels "within" or "in" the substrate layer of a multi-layered printed circuit board. A first optical channel is formed in a first substrate, and a second optical channel is formed in a second substrate. The two substrates are stacked together and the channels communicate through vias or switches.

Claim Rejections: 35 USC § 102(b)

Claims 1 and 50 are rejected under 35 USC § 102(b) as being anticipated by USPN 5,432,873 (Hosoya). These rejections are traversed.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See MPEP § 2131, also, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Since Hosoya neither teaches nor suggests each element in claims 1 and 50, these claims are allowable over Hosoya.

Claim 1

Independent claim 1 recites numerous elements and/or recitations that are not taught in Hosoya. Some examples are provided below.

As one example, claim 1 recites that the channel is created "within a planar layer in a first substrate of a multi-layered printed circuit board (PCB) and within a planar layer in a second substrate of the multi-layered PCB" (emphasis added). Hosoya discloses that the optical waveguides are formed on top of a substrate, not within the substrates of a multi-layered printed circuit board. Figures 1 and 2 of Hosoya show a substrate 6 that has two waveguides 8 and 11 formed on top of the substrate 6. Again, nowhere does Hosoya state that the waveguides are formed in substrate 6. Further, nowhere does Hosoya state that the waveguides are formed in substrates of a multi-layered printed circuit board.

Anticipation under section 102 can be found only if a single reference shows exactly what is claimed (see *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985)). For at least these reasons, claims 1 and 50 are allowable over Hosoya.

As another example, claim 1 recites that the first and second substrates are stacked together in a multi-layered printed circuit board. Hosoya does not teach two substrates that are stacked with a channel formed in both the first and second substrates of a multi-layered PCB. Figs. 1 and 2 in Hosoya show a single substrate 6 with a first waveguide 8 formed in thin layer 7 and a second waveguide 11 formed in thin layer 10. Again, Hosoya does not disclose two stacked together to form a multi-layered PCB as recited in claim 1.

For a prior art reference to anticipate under section 102, every element of the claimed invention must be identically shown in a single reference (see *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990)). For at least these reasons, claims 1 and 50 are allowable over Hosoya.

Response to Examiner's Arguments

The Examiner argues that the term "substrate" is a very broad term that refers to any layer underneath another layer (see Final OA at p. 9). Applicants respectfully disagree since the interpretation of the Examiner is so broad as to be contrary to the express teachings in Hosoya.

In the field of optical switches and printed circuit boards, the term "substrate" has a distinct meaning to one skilled in the art. Hosoya repeatedly uses the term "substrate" in accordance with the meaning of this term. Specifically, Hosoya teaches optical switches with optical waveguides that are formed on top of a "substrate" not within the substrates. Figures 1 and 2 of Hosoya show a substrate 6 that has two waveguides 8 and 11 formed on top of the substrate 6. Notice that Hosoya even labels his layers as "substrate" layer (i.e., reference number 6) and cladding layer (i.e., reference number 9).

Optical switches are formed in a very precise manner using layers. Each layer (i.e., the substrate layer, the cladding layer, etc.) perform a very specific function to enable optical transmission through channels. One skilled in the art of optical switches uses these specific terms to describe and understand the technology.

The Examiner intends to call cladding layers and thin film layers in Hosoya as being the substrate layers. This interpretation is so broad that it is contrary to the express teachings in Hosoya but also repugnant and contrary to the use of such terms in the art.

Law on Claim Interpretation

According to MPEP § 2111.01, the words of a claim must be given their "plain meaning." Appellants acknowledge that claims must be given their broadest interpretation during patent examination. However, this interpretation must be a "**reasonable interpretation consistent with the specification**" (see MPEP 2111: emphasis added). Appellants specification and Hosoya repeatedly uses the term

"substrate" in a manner consistent with the plain meaning of this term. Appellants respectfully ask the Board of Appeals to interpret the word "substrate" in a reasonable manner consistent with the specification and use of this term to one skilled in the art.

Claim 50

Claim 50 recites switching the switch between an opaque state that prevents passage of an optical signal and a transparent state that permits passage of the optical signal. Thus, claim 50 recites a switch that has two different states. The Examiner argues that these different states are shown in Hosoya at column 7, lines 1-25. Applicants respectfully disagree.

Column 7, lines 1-25 in Hosoya teach discuss how to form a thin film layer (see reference numbers 7 and 10 in Figs. 1-2) in an optical switch. This section also discusses transmitting light through the waveguide and observing the output of power on the other side of the waveguide. Nowhere does this section teach or even discuss that the optical switch has an "opaque state" preventing passage of light or a "transparent state" permitting passage of optical light. This section of Hosoya is completely silent on permitting and preventing passage of light using such states.

Claim Rejections: 35 USC § 103(a)

Claims 2, 4-5, and 9-11 are rejected under 35 USC § 103(a) as being unpatentable over Hosoya in view of US publication number 2003/0118310 (Steinberg). As shown above in section, Hosoya does not teach or suggest all the elements in independent claim 1. Steinberg fails to cure these deficiencies. For at least these reasons, dependent claims 2, 4-5, and 9-11 are allowable over Hosoya in view of Steinberg.

Claim Rejections: 35 USC § 103(a)

Claims 2-5 and 12-15 are rejected under 35 USC § 103(a) as being unpatentable over Hosoya in view of USPN 6,624,077 (White). As shown above in section, Hosoya does not teach or suggest all the elements in independent claim 1. White fails to cure these deficiencies. For at least these reasons, dependent claims 2-5 and 12-15 are allowable over Hosoya in view of White.

Claim Rejections: 35 USC § 103(a)

Claims 2, 6-9, and 14 are rejected under 35 USC § 103(a) as being unpatentable over Hosoya in view of US publication number 2001/0026670 (Takizawa). As shown above, Hosoya does not teach or suggest all the elements in independent claim 1. Takizawa fails to cure these deficiencies. For at least these reasons, dependent claims 2, 6-9, and 14 are allowable over Hosoya in view of Takizawa.

Claim Rejections: 35 USC § 103(a)

Claims 16, 18-19, and 21-23 are rejected under 35 USC § 103(a) as being unpatentable over USPN 6,624,077 (White) in view of USPN 6,693,736 (Yoshimura). These rejections are traversed.

Independent claim 16 recites one or more elements that are not taught or suggested in White in view of Yoshimura. These missing elements show that the differences between the combined teachings in the art and the recitations in the claims are great. As such, the pending claims are not a predictable variation of the art to one of ordinary skill in the art.

Claim 16 recites providing first and second substrates in respective first and second layers. Each layer has a channeled face defining a channel "formed in" the substrate. The layers are placed together to form a channel in a multi-layered printed circuit board. White does not teach or suggest these elements.

Fig. 2A in White shows a waveguide 200 having a top substrate 203 and a bottom substrate 204. Two cladding layers 205 and 207 are disposed between the two substrates. A conductive core 210 is disposed in the cladding layers, not in the substrates. White expressly teaches that the channels are formed in a cladding layer, not in a substrate layer: "Cladding layer 206 has a trench or channel 212 of a substantial semi-circular cross section formed therein" (White at column 4, lines 61-63).

The differences between the claims and the teachings in the art are great since the references fail to teach or suggest all of the claim elements. As such, the pending claims are not a predictable variation of the art to one of ordinary skill in the art.

For at least these reasons, the claims 16, 18-19, and 21-23 are allowable over the art of record.

As yet another example, claim 16 recites vias through first and second layers of the multi-layered printed circuit board "to connect composite channels." Nowhere does White in view of Yoshimura teach or even suggest such a recitation. The Examiner argues that this recitation is taught in Yoshimura in Figures 1-2 (see Final OA at p. 7). Applicants respectfully disagree.

Figs. 1 and 2 in Yoshimura teach an optical circuit having a waveguide 11, a substrate 1, a clad layer 13, and a light source 5. Notice that nowhere does Yoshimura teach or even suggest that vias connect "composite channels with different optical pathways." Yoshimura does not show composite channels. Instead, the channels in Yoshimura are individually provided in the layers. As recited in claim 1, composite channels are formed when two planar layers with complimentary channels are placed opposite each other.

The differences between the claims and the teachings in the art are great since the references fail to teach or suggest all of the claim elements. As such, the pending claims are not a predictable variation of the art to one of ordinary skill in the art.

For at least these reasons, the claims 16, 18-19, and 21-23 are allowable over the art of record.

Response to Examiner's Arguments

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In the field of optical switches and printed circuit boards, the term "substrate" has a distinct meaning to one skilled in the art. White repeatedly uses the term "substrate" in accordance with the meaning of this term. Specifically, Fig. 2A in White shows a waveguide 200 having a top substrate 203 and a bottom substrate 204. Two cladding layers 205 and 207 are disposed between the two substrates. A conductive core 210 is disposed in the cladding layers, not in the substrates. White expressly teaches that the

channels are formed in a cladding layer, not in a substrate layer: "Cladding layer 206 has a trench or channel 212 of a substantial semi-circular cross section formed therein" (White at column 4, lines 61-63). Notice that White even labels his layers as "substrate" layer (i.e., reference numbers 204 and 203) and cladding layers (i.e., reference numbers 206 and 207).

Optical switches are formed in a very precise manner using layers. Each layer (i.e., the substrate layer, the cladding layer, etc.) perform a very specific function to enable optical transmission through channels. One skilled in the art of optical switches uses these specific terms to describe and understand the technology.

The Examiner intends to call cladding layers in White as being the substrate layers. This interpretation is so broad that it is contrary to the express teachings in White but also repugnant and contrary to the use of such terms in the art.

Law on Claim Interpretation

According to MPEP § 2111.01, the words of a claim must be given their "plain meaning." Appellants acknowledge that claims must be given their broadest interpretation during patent examination. However, this interpretation must be a "**reasonable interpretation consistent with the specification**" (see MPEP 2111: emphasis added). Appellants specification and White repeatedly uses the term "substrate" in a manner consistent with the plain meaning of this term. Appellants respectfully ask the Board of Appeals to interpret the word "substrate" in a reasonable manner consistent with the specification and use of this term to one skilled in the art.

Claim Rejections: 35 USC § 103(a)

Claims 17 and 20 are rejected under 35 USC § 103(a) as being unpatentable over USPN 6,624,077 (White) in view of USPN 6,693,736 (Yoshimura) and 2003/0118310 (Steinberg). These rejections are traversed. As shown above, White and Yoshimura do not teach or suggest all the elements in independent claim 16. Steinberg fails to cure these deficiencies. For at least these reasons, dependent claims 17 and 20 are allowable over White in view of Yoshimura and Steinberg.

CONCLUSION

In view of the above, Applicants respectfully request the Board of Appeals to reverse the Examiner's rejection of all pending claims.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. 832-236-5529. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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VIII. Claims Appendix

1. A method of forming an optical communication path, comprising:

a) creating a channel within a planar layer in a first substrate of a multi-layered printed circuit board (PCB) and within a planar layer in a second substrate of the multi-layered PCB;

b) forming at least a portion of an optical path within the channel of the first and second substrates, the first and second substrates being stacked together in the multi-layered PCB; and

c) optically coupling with a switch the channel in the first substrate with the channel in the second substrate.

2. The method of claim 1 wherein step a) further comprises creating the channel using a selected one of a chemical, mechanical, and a thermal process to remove planar layer material.

3. The method of claim 1 wherein step a) comprises molding the planar layer with the channel.

4. The method of claim 1 wherein step a) further comprises:

i) lithographically defining a location of the optical path on a face of the planar layer; and

ii) etching the planar layer along the defined location of the optical path to create the channel.

5. The method of claim 1 wherein step b) further comprises filling the channel with an optical core medium.

6. The method of claim 1 wherein step b) further comprises:

i. depositing a first cladding portion within the channel; and

ii. depositing an optical core medium within the channel; and

iii. depositing a second cladding portion over the optical core medium.

7. The method of claim 6 wherein one of the first and second cladding portions has an index of refraction less than an optical core medium index of refraction.

8. The method of claim 6 wherein at least one of the first and second cladding portions is optically reflective along a side adjacent the optical core medium.

9. The method of claim 1 further comprising:

i. depositing a cladding portion within the channel; and

ii. depositing an optical core medium within the channel.

10. The method of claim 9 wherein the cladding portion has an index of refraction less than an optical core medium index of refraction.

11. The method of claim 9 wherein the cladding portion is optically reflective along a side adjacent the optical core medium.

12. The method of claim 1 wherein the planar layer is a selected one of a conductor, nonconductor, and semiconductor layer.

13. The method of claim 1 wherein walls of the channel have a lower index of refraction than that of the optical core medium.

14. The method of claim 1 wherein the optical path is substantially non-cylindrical.

15. The method of claim 1, further comprising:

c) forming an electrical trace supported by the planar layer.

16. A method of forming an optical communication path, comprising:

a) providing a first substrate with a first planar layer having a channeled face defining a first channel formed in the first substrate;

b) providing a second substrate with a second planar layer having a complementary channeled face defining a second channel formed in the second substrate;

c) placing the first and second planar layers such that the first and complementary second channels oppose each other to form a composite channel defining the optical path in a multi-layered printed circuit board; and

d) providing vias through the first and second planar layers to connect the composite channel with different optical pathways extending through different vertically stacked layers of the multi-layered printed circuit board.

17. The method of claim 16 further comprising applying a reflective coating to the first and second planar layers.

18. The method of claim 16 further comprising depositing an optical core medium within the first and second channels.

19. The method of claim 16 further comprising filling the composite channel with an optical core medium.

20. The method of claim 16 further comprising applying a reflecting coating over the first and second channels.

21. The method of claim 16 wherein the first and second channels have a semi-circular cross-section.

22. The method of claim 16 wherein one of the first and second channels is created through a selected one of a chemical, mechanical, or thermal process applied to a planar layer.

23. The method of claim 16 wherein one of the first and second planar layers is molded with its respective channel.

24. – 49. (canceled)

50. The method of claim 1 further comprising:

d) switching the switch between an opaque state that prevents passage of an optical signal and a transparent state that permits passage of the optical signal.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.